REMARKS

Reconsideration of this application is respectfully requested in view of the foregoing amendments and the following remarks.

I Response to Rejections Under 35 U.S.C. § 112

The rejection under 35 U.S.C. 112, second paragraph, has been addressed by amending line 1 of claim 1 to positively recite "a flat display panel," thereby providing proper antecedent basis for subsequent recitations of "the flat display panel."

In addition, the claims and specification have been amended to correct various minor grammatical and idiomatic errors and to improve readability. Because the changes are all formal in nature, it is respectfully submitted that they do not involve "new matter."

II. Response to Rejections Under 35 U.S.C. § 102

The rejection of claims 1-8 under 35 U.S.C. § 102(b) as being anticipated by Aoki et al (6,177,916) is respectfully traversed on the grounds that the Aoki patent fails to disclose or suggest a flat panel display driving circuit having a plurality of switch units disposed between video signal lines 211, 212, 213 for providing analog video signals. The switch units 14, 34, 44, 54, 64, and 74 of Aoki are all disposed below the video buses or signal lines 13, 33, 43, 63, and 73, which is exactly the arrangement discussed in the background section of the present application.

As shown in FIG. 2a of the present application, there are three video signal lines 211, 212, 213, and three switches 221, 222, 223 disposed between the red signal line 212 and the green signal line 213. As a result of this arrangement, recited in each of the original claims, parasitic capacitances which come from crossover points can be reduced, as depicted in FIG. 2b, in comparison with the prior driving circuit, as shown in FIG. 1, in which switches 111, 112, 113 are all disposed below signal lines 121, 122, 123, i.e., between signal lines 121, 122, 123 and active area (display area) 131.

Like the prior art driving circuit shown in Fig. 1 of the present application, the driving circuit of Aoki includes video buses (video signal lines) 13, 33, 43, 63, 73 that are all disposed above the analogue switches 14, 34, 44, 54, 64, 74. In Aoki, none of analog switches 14, 34, 44, 54, 64, 74 is disposed between the video buses 13, 33, 43, 63, 73. This arrangement in Aoki suffers from having an excessive quantity of parasitic capacitances, resulting in unwanted power consumption and poor picture quality. Although Aoki does attempt to reduce parasitic capacitances, the parasitic capacitances to be reduced come from the overlap between the output signal line 17 (of timing signal generator circuit 11) and the video buses 13, which is different from that of the present application, in which any parasitic capacitance comes from the crossover between the analog switches 111, 112 113 and the signal lines 121, 122, 123.

Instead of placing signal lines between switches as in the claimed invention,
Aoki tries to reduce parasitic capacitance loads by a structure in which output lines

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18 of the buffer circuits 12, which are connected with each other, are connected to

the gates 110 of the analog switches 14, and the video busses 13 are connected to

the analog switches 14 through output lines 19 (column 3 line 65 to column 4 line

10). This structure for reducing parasitic capacitance loads is clearly different from

that of the present application in which the switch units are disposed between the

signal lines to reduce parasitic capacitances which comes from crossover points.

Thus, applicant respectfully submits that Aoki neither discloses nor suggests the

driving circuit of the claimed invention, whether considered individually or in

combination with any other reference of record, and therefore withdrawal of the

rejection of claims 1-8 under 35 U.S.C. § 102(b) is accordingly requested.

CONCLUSION

In view of the foregoing remarks, reconsideration and allowance of the

application are now believed to be in order, and such action is hereby solicited. If

any points remain in issue that the Examiner feels may be best resolved through a

personal or telephone interview, the Examiner is kindly requested to contact the

undersigned attorney at the telephone number listed below.

Respectfully submitted,

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By:

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Date: October 3, 2006

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